ELECTRICAL CHARACTERISTICS OF GRAPHENE BASED TRANSISTORS

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Graphene has recently emerged as a potential candidate material for nanoelectronics due to its electronic properties[1]. Geometrically is a monolayer of carbon atoms tightly packed into a 2D honeycomb lattice known to be a zero-gap material that could be fabricated using mechanical exfoliation[2] and epitaxial growth[3]. Interestingly, graphene could be patterned in nano-ribbons, using planar technologies as electron beam lithography and etching[3-4], having properties theoretically predicted to range from metallic to semiconducting depending on their width and edges[5]. This band-gap tuning capability and the possibility of large-scale integration using planar technologies open a route towards an all-graphene electronic nanodevices and circuits. Notably, recent studies[2] reported mobilities for electrons and holes in graphene of the order of 10^4 $cm^2/V{\cdot}s$. However, mobility for GNRs is expected to have smaller values than graphene, with an inverse dependence with the band gap[6], but conclusive experimental studies still lack. At this early state of development of GNR technology it seems timely to develop models of building blocks helping to conduct experiments in the same line as previously reported for carbon nanotube based devices[7-8]. This work presents an easy to implement model for analyze or design the current-voltage (I-V) characteristics of GNR-FETs in connection with physical parameters, such as GNR width (W) and gate insulator thickness (t_{ins}), and electrical parameters, such as SB height (φ_{SB}). The proposed approach prevents the computational burden that self-consistency implies by using a closed-form electrostatic potential from Laplace's equation. This simplification yields accurate results compared with self-consistent results from NEGF method[9] in the relevant limit dominated by the GNR quantum capacitance (C_{GNR}). Note that it appears to be the interesting case for advanced applications because the ability of the gate to control the potential in the channel is maximized. The presented model is intended to assist at the design stage as well as for quantitative understanding of experiments involving GNR-FETs.

References:

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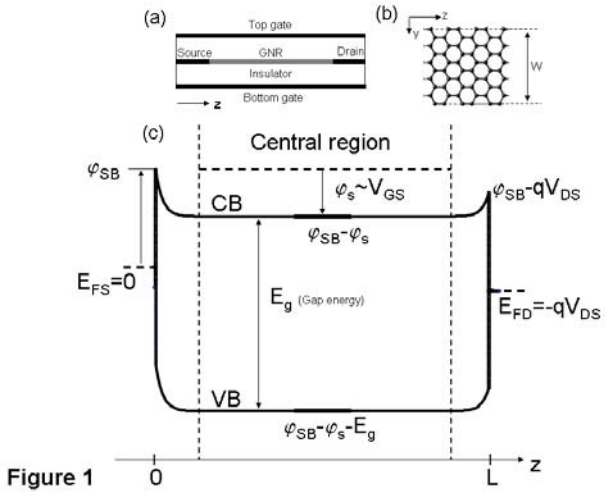

Fig.1: *Geometry and band diagram of the GNR-FET: (a) cross-section, (b) top view of the armchair shaped edge GNR forming the channel, and (c) sketch of the spatial band diagram along the transport direction.*

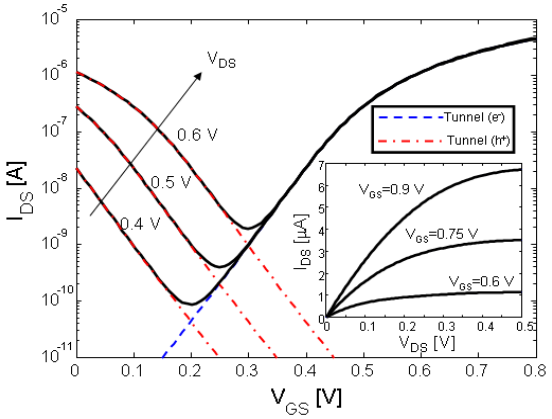

Fig.2: *Transfer and output characteristics (inset) for the nominal GNR-FET. Decomposition of the total current in electron and hole tunneling contributions are shown.*

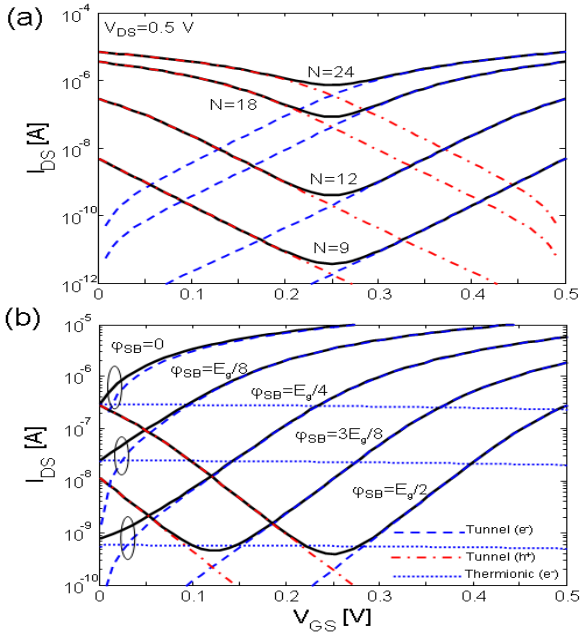

Fig.3: Influence of the GNR width (a) and SB height (b) in the transfer characteristics.