Efficient MVL Circuit Design with Use of p-CNTFETs and n-CNTFETs

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Introduction

As the miniaturization of silicon based circuits reaches its physical limits, the exigency of substitute technologies emerges. Special characteristics of CNT such as high mobility of electrons, ballistic transport and high I_{on}-I_{off} ratio, has introduced it as an appropriate successor to silicon MOSFET. Whereas the threshold voltage cannot be decreased deliberately due to the scaling limitations of MOSFETs, in CNTFETs different threshold voltages can be obtained simply by defining different nanotube diameters because the threshold voltage is in reverse proportion with the nanotube diameter [1]. This feature of carbon nanotubes has been exploited in implementation of multiple valued logic (MVL) circuits. One of the principal ways in MVL circuit implementation is by using basic operators such as tsum, literal, min and max. In [2] we introduced a new approach for ternary Galois field design that employed different paths to obtain different logic levels and showed that this approach is more efficient than using basic MVL operators. In [3] we presented another design for Galois field which employed sharing paths method to obtain output logical levels. In this paper we propose a CNTFET design for multiplication and addition circuits that not only take advantages of these two but also further reduces the number of transistors by the idea of bridging a resistor between CNTFETs.

The Circuits Functionality

In this section we specify the proposed design of ternary multiplication and addition operators using CNTFETs. In our implementation, supply voltage has been chosen to be 1.5V (V_{DD}) which ensures sufficient static noise margin. This implementation consists of both p-CNTFETs and n-CNTFETs with two different diameters, 1.4nm and 0.5nm. These nanotube transistors have the corresponding threshold voltages V_{th1} = 300mV and V_{th2} = 840mV respectively. Input voltage values for logics 0, 1 and 2 are $V_{in} < V_{th1}$, $V_{th1} < V_{in} < V_{th2}$ and $V_{th2} < V_{in}$ respectively. Speaking in the ternary logic, if output voltage lies between 0 to $\frac{V_{DD}}{3}$ then the output will be logic 0, and in case that output voltage lies between $\frac{V_{DD}}{3}$ to $\frac{2V_{DD}}{3}$ then the output will be logic 1, and if the output voltage is greater than $\frac{2V_{DD}}{3}$ then the output will be logic 2.

Figure 1 shows the circuit realization of addition and multiplication operations. In both circuits, output is set to logic 0 using the pull up network. In the pull down network, resistor paths set the circuit output to logic 1 by voltage division and the non-resistor paths set the output to logic 2. According to the special arrangement of CNTFETs and their specific threshold voltages, in multiplication circuit, fig.1 (a), if at least one of the input values is zero then all the transistors will go off and the circuit output will be zero. When the output is to be logic 1, the voltage is divided between R and R_1. For example if inputs a=b=2 then the transistors T_1 and T_6 goes on and the output voltage range is as expressed by Eq.1. Since the R_1 plays a rule only when the output is logic 1, by solving the Eq.1 the relation between R and R_1 is obtained by Eq.2. In cases that inputs are a=1, b=2 or when a=2, b=1, then the transistors T_1,T_2,T_3 or T_4,T_5,T_6 will go on and the non-resistor path will be active. Hence the Z will be completely discharged and this brings the output of the circuit to logic 2. The functionality of addition circuit, fig.1 (b), can be analyzed in a similar way.

$$\frac{V_{DD}}{3} \leq V_{DD}\frac{R_1}{R+R_1} \leq \frac{2V_{DD}}{3} \quad \text{(Eq. 1)}$$

$$\frac{R}{2} \leq R_1 \leq R \quad \text{(Eq. 2)}$$

Conclusion

In this paper we have introduced an efficient novel design for CNTFET ternary multiplication and addition circuits which by using resistor(s) (R_1) between transistors as the bridge, makes it possible to reduce the total number of transistors. The proposed approach can be applied to design efficient higher radix MVL circuits.

In [4] multiplication and addition circuits have been designed by use of CNTFET multiplexers. The techniques employed in our proposed design along with exploiting the relationship between V_{th} and nanotube diameter, have made it an efficient design which uses the minimum number of transistors. The number of transistors in multiplication and addition circuits of [4] is 16 each, but in our design these numbers are 8 and 14 respectively. It should be noted that according to [1], the NOT gate is made up of two CNTFETs.

References:

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Figures:

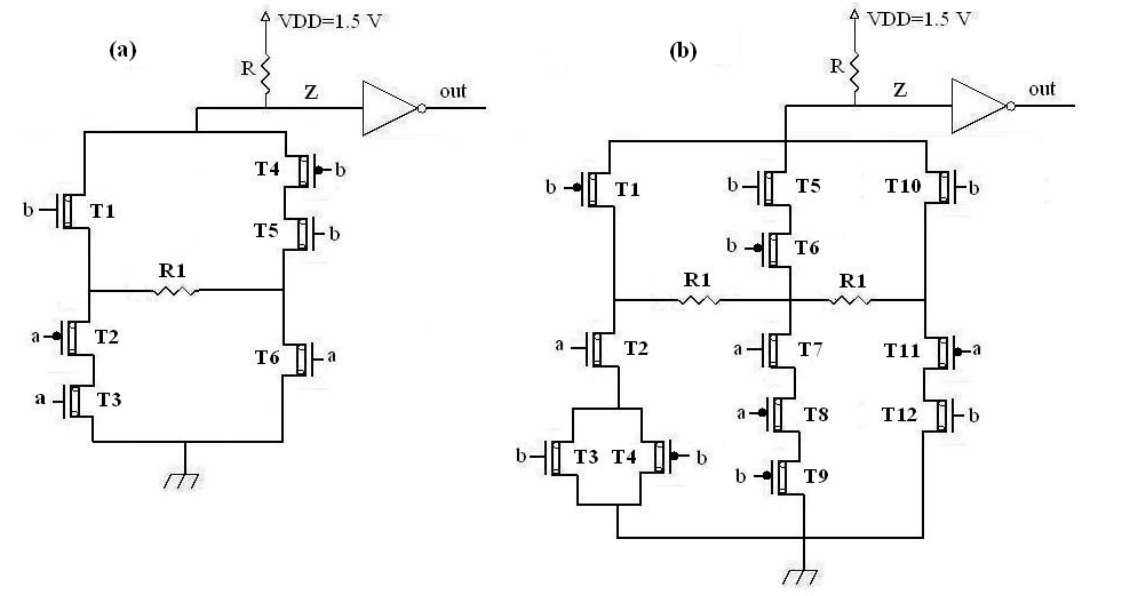

Fig.1. (a): GF(3) multiplication circuit using CNTFETs. The diameter of transistors T1 and T6 is 0.5nm and the diameter of the other transistors is 1.4nm. Resistors R and R_1 are 100kΩ. (b): GF(3) addition circuit using CNTFETs. The diameter of transistors T1, T2, T3, T4, T10 and T11 is 0.5nm and the diameter of the other transistors is 1.4nm. Resistor