Simulations of a Planar Silicon Tunnel Field-Effect Transistor

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As planar metal-oxide-semiconductor field-effect transistors (MOSFETs) are scaled to the nanometre regime, their sub-threshold swing (SS) characteristics significantly degrade. This degradation causes a high power consumption limiting the performance of low power transistors in digital applications. Tunnelling-FETs (TFETs) are considered a promising solution to overcome the poor performance of MOSFETs in the sub-threshold region (leakage current (I_{OFF}) and SS) [1] by surpassing the fundamental limit of MOSFETs of 60 mV/dec at room temperature. The on-current (I_{ON}) of TFETs depends on the distance between the conduction and valence band because the I_{ON} arises from a band-to-band tunnelling (BTBT) process with low efficiency. Thus the TFETs suffer from a low I_{ON} [2]-[3]. In Ref. [3], a new device structure is proposed to overcome the low I_{ON} issue by adding an extra layer between the gate-dielectric and the p-i-n junction in order to increase the tunnelling area. The aim of this work is to investigate and optimise the performance of a TFET based on the experimental device [3]. The n-type Si TFET has a gate length of 1 µm shown in Fig. 1. The epi-layer and the SOI have an intrinsic doping of 1.0×10^{15} cm^{-3}, the p-type source has a concentration of 3.7×10^{19} cm^{-3} and the n-type drain of 2.7×10^{20} cm^{-3}. The work function of the metal gate is 4.8 eV. All the simulations have been performed using Silvaco ATLAS [6] accounting for both the local and non-local BTBT, for the band-gap narrowing, and the thermionic emission transport model. Fig. 2 shows the I_D-V_G characteristics at a drain bias of 1.0 V comparing simulations with experimental data with a very good agreement at large gate biases. The simulations allow to optimise the device architecture since I_{OFF} increases dramatically with a drain-to-gate distance (D) while I_{ON} shows a minimal change.

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References

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Figures

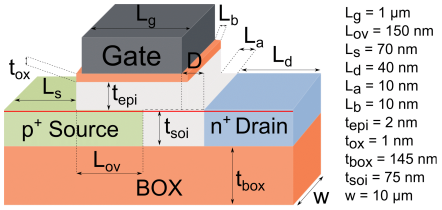

Figure 1: Schematic of the TFET with the corresponding dimensions. The z-direction is assumed to be a 10 µm wide.

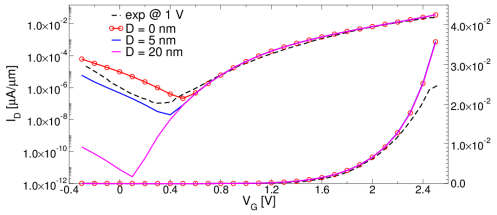

Figure 2: I_D-V_G characteristics on both linear (right) and logarithmic (left) scales at a high drain bias of 1.0 V.