Nanoscale and device level degradation of Hf/SiO_2 gate stacks in CMOS electronic nanodevices.

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The progressive increase of the tunnel gate current in SiO_2 based MOS nanodevices [1], due to the reduction of the gate oxide thickness, has led to a search for alternative materials with a higher dielectric constant. It must be considered, however, that, to form a good quality interface (low defect density) with Si, an ultrathin SiO_2 film is grown between the high-K material and the Si substrate, so that the gate dielectric is actually formed of a high-K/SiO_2 stack. Since the SiO_2 interfacial layer reduces the lowest achievable equivalent oxide thickness (EOT) [1], a SiO_2 layer as thin as possible is required, although it is difficult to obtain thicknesses lower than 0.5 nm. Before the definitive replacement of SiO_2 in commercial IC's, the electrical properties and reliability of these gate stacks must be studied. A crucial issue that affects their reliability is the generation of defects during the degradation stage, when the structure is submitted to an electrical stress. At this point, the particular role of each of the stack layers still remains to be determined. In this work, standard device level and nanoscale electrical tests have been carried out to evaluate the influence of the high-k and interfacial SiO_2 layers on the degradation of high-K gate stacks (HfO_2/SiO_2).

At device level, the degradation of MOS capacitors subjected to static and dynamic electrical stresses has been analysed, to evaluate the effect of a polarity change in the degradation of the high-K stack. Measurements were performed using standard equipment for electrical characterization at wafer level. The studied samples were MOS capacitors with n-type substrate and 3.5 nm thick HfO_2. Two different interfacial SiO_2 thicknesses (1 and 1.8 nm) have been investigated, corresponding to a structure EOT of 1.5 and 2.3nm, respectively. The degradation of the samples was determined from a stress and sense procedure. The electrical stresses consisted in a positive Constant Voltage Stress (CVS), negative CVS, positive unipolar or bipolar stress, applied during a predetermined time. After the stress, a ramped voltage stress (RVS) between -1.5V to 1.5V was applied, to measure the current density after the different stresses (measured at 0.75V). The change in the current density is indicative of the stack degradation.

Figure 1 shows the evolution of the current density with the stress time. This figure suggests that the degradation depends on the stress applied. Positive CVS provokes the larger degradation (higher current density increment). Bipolar and unipolar stresses produce less degradation than positive stress and very similar between them. Finally the smaller degradation is obtained for the negative CVS. These results are in agreement with the ones presented by other authors in the literature [2] remarking that in high-K stacks negative stress provokes less damage than the positive stress, probably due to the asymmetries in the band diagram. For the bipolar case, the change of stress polarity could produce some influence in the traps or in the species related to the degradation, leading to a decrease in the damage of the stack compared to the positive CVS case. The similar evolution of the degradation with the stress time for the bipolar and unipolar cases seems to indicate that the degradation induced during the negative cycle in the bipolar case is comparable to the effect of the off state during the unipolar stress. On the other hand, the degradation induced in the stack depends on the thickness of the SiO_2 interfacial layer. Figure 1 shows that for all the applied stresses (positive, negative, bipolar, unipolar stress) the degradation for the 1 nm SiO_2 thickness is always larger than for 1.8 nm SiO_2 thickness (higher current density increments are measured for 1 nm SiO_2 thickness).

A nanoscale characterization of high-k/SiO_2 degradation has been also carried out, using a Conductive Atomic Force Microscopy (C-AFM), since it has been demonstrated to be very useful in the study of SiO_2 and high-k electrical properties [3-5] at the nanoscale. This analysis (areas of ~300nm^2 can be investigated) reveals details that can be masked during standard tests. However, for some measurements, the electrical capabilities of the C-AFM are not enough. To overcome this limitation, in this work, a prototype of C-AFM with enhanced electrical performance (ECAFM) [6] has been used to investigate the effect of the electrical stress on the conduction of ultra-thin HfO_2/SiO_2 gate stacks. In the nanoscale experiments, bare gate stacks with a 2.5 or 4.5nm thick HfO_2 layer grown on a 0.6nm SiO_2 interface layer have been investigated. The electrical behaviour of these stacks has been compared to 0.6nm nominal thick SiO_2 layers. With the ECAFM, ramped voltage stresses (RVS) have been applied at the nanoscale, using the tip of the microscope as gate electrode.

We have started investigating the electrical conduction of high-k gate stacks, which will be compared to that observed in SiO_2 layers. Fig. 2 shows typical I-V curves measured on a (I) 0.6nm nominal thick SiO_2 layer (which shows the Direct Tunneling current through the oxide) and (II) and (III) high-k gate stacks with a HfO_2 layer of 2.5 and 4.5nm respectively. In the case of high-k stacks (curves II and III), for low gate voltages ($V_G <$ 7V), fresh I-V characteristics show different conduction regimes [3]: a region where current increases several orders of magnitude (A) and a plateau region (B), which have been attributed, respectively, to carrier injection through a triangular HfO_2 barrier (and, of course, through the SiO_2 barrier) and to carrier injection at energies above the barrier of HfO_2 (inset Fig. 2). The transition between both regimes takes place when the barrier height equals the potential drop across the SiO_2. Beyond region (B) (V_G>7V), the current progressively increases in both samples (SiO_2 and high-k gate stacks) reaching the so called regime (C).

The effect of the stress on the different layers of the high-k gate stack has been investigated from series of RVS applied on fixed sites. Fig. 3 shows a sequence of I-V characteristics registered when the end voltage of the RVS is at the beginning (low field stress) of the plateau region. Note that the plateau region starts at lower voltages as the stress proceeds, indicating a progressive increase of the electrical conduction (related to the degradation) of the gate stack. Moreover, sometimes, switchings are observed (see Fig. 3), which have been related to the generation of defects and to the trapping/detrapping of charges in the generated traps [5]. However, the current registered in the plateau region (when conduction is controlled by the SiO_2 layer) remains nearly constant. Therefore, from these results, one can conclude that, at low field stresses, the progressive increase in the electrical conduction of the stack can be mainly related to the degradation of the high-k film instead of the SiO_2 layer. The electrical properties of high-k gate stacks have also been investigated when the structure is subjected to high field stresses (RVS with final voltage beyond the plateau region, not shown). In this case, regime C is reached and the current noisily increases until a current jump occurs, leading to the stack breakdown (BD). Since this regime is only observed when the injection is controlled by the SiO_2 layer, this noisy behaviour can be attributed to the degradation and BD of the SiO_2 oxide.

In this work, the degradation of HfO_2/SiO_2 gate stacks has been investigated at device and nanoscale levels. At device level, gate stacks with different SiO_2 thickness have been subjected to static and dynamic (positive unipolar and bipolar) stresses, using standard characterization techniques, to analyse the evolution of the dielectric degradation for the different stresses and SiO_2 thickness. For the same stress time, positive CVS produces the larger degradation, bipolar and unipolar show less degradation and negative CVS the lowest. The similar evolution of the bipolar and unipolar cases could indicate that the negative cycle during bipolar stress is comparable to the off state of the unipolar one. For the same stress condition, the degradation of high-k stacks is larger as the thickness of the SiO_2 interfacial layer decreases. On the other hand, an ECAFM has allowed to separately investigate the effect of the electrical stress on the SiO_2 and HfO_2 layer of a high-k gate stack. The results show that, at low voltages, the electrical properties of the gate stack are determined by the HfO_2 film. In particular, as the stress proceeds, an increase in conductivity is observed, related to the generation of defects in the HfO_2 layer. Trapping and detrapping from these defects lead to switching in the electrical characteristics. However, at high voltages, electrical conduction and BD is controlled by the SiO_2 interface film.

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Figures:

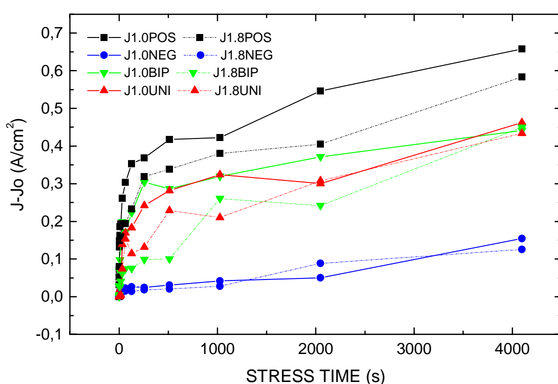

Fig.1. Comparison between J-Jo values for HfO_2/SiO_2 stacks with 1 nm and 1.8 nm SiO_2 thickness subjected to different static and dynamic stresses as a function of the stress time.

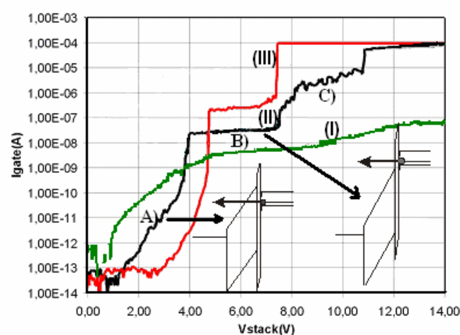

Fig.2. I-V curves obtained with the ECAFM in a fresh location of a (I) SiO_2 layer and (II) 2.5nm and (III) 4.5nm thick gate stack.

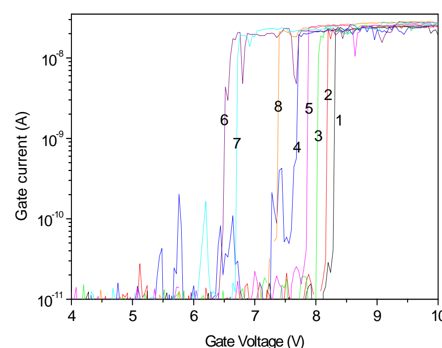

Fig.3. ECAFM I-V curves measured during a RVS sequence in which the conduction is controlled by the HfO_2 layer.