Variation and modeling of MOS transistor characteristics under the effects of the gate dielectric degradation and final breakdown

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The progressive scaling of SiO_2 thickness in MOS devices has produced the appearance of several failure mechanisms that affect their reliability. Nowadays, the final oxide dielectric breakdown (BD) and its previous degradation process are very interesting subjects for the scientific community especially for oxide thickness below 3 nm [1]. In this sense, several works in the literature are devoted to the influence of the degradation and BD of the oxide on the performance of circuits. Although it seems that the reliability predictions are overestimated and that the devices and circuits can still work after an important level of degradation, this question is still not clear. To advance in this study it is necessary the development of transistor models for circuit simulators to predict the effect of the degradation and BD on circuit functionally. In this sense, it is very important that the device parameters of the model include the effect of the oxide degradation and BD to simulate a more realistic effect of these failure mechanisms on circuit performance. In this work, experimental transistor curves have been modeled taking into account the variation of the model parameters after the final BD, which is called hard breakdown (HBD) and also during the previous oxide degradation process. For the first case, the transistor curves have been fitted using a recently developed BD MOSFET model which includes the effect of the dielectric breakdown on the transistor parameters. The model consists in the well known nth power MOSFET model [2] plus an additional voltage driven current source to take into account the additional current path due to oxide breakdown (Fig. 1). This current source follows the power law formula $I=KV^P$ [3], which has been shown to be useful in the modelling of CMOS inverters [4]. The nth power law model is a simple model and only 6 parameters are necessary to determine the transistor output characteristics. On the other hand, the influence of the oxide degradation process before the oxide BD on the transistor functionality has also been analysed and the experimental transistor curves fitted with the BSIM4 model, whose parameters are extracted after the oxide degradation. Although this approach would be the most accurate, it needs a larger number of parameters than the previous one and the extraction of the parameters is more complicated.

Experimental measurements have been performed to analyse the influence of oxide HBD on transistor characteristics. Constant voltage stresses between 3 and 3.5V were applied to the gate of nMOSFETs (1.5V bulk technology, W/L ratio 20μm/0.6μm and oxide thickness of 2 nm) with the other terminals grounded. The stress duration was large enough to provoke oxide HBD (I_G current of the order of mA). The gate (I_G), drain (I_D) and source (I_S) currents through the transistor have been measured before and after HBD. The BD path position along the channel has been determined by evaluating the ratio I_D/I_D+I_S [5] and in this first part of the work we have considered only BD locations between gate and source (source HBD) or gate and drain (drain HBD) overlap regions because these are the worst cases. The parameters of the nth power model were extracted by fitting the experimental I_D-V_{DS} transistor curves (with V_{GS} as a parameter and V_{BS}=0). The post-BD drain and source currents were fitted to the BD power law model to obtain the K and p parameters of the drain and source currents respectively. Figure 2 shows the post-BD I_D-V_{DS} experimental characteristics of two nMOSFETs with drain and source HBD with similar hardness. The characteristic of a fresh transistor is also shown for comparison. Different behaviours of the nMOSFET can be observed depending of the BD position which indicates that other parameters apart from the gate current are affected. After drain HBD (up triangles), a negative I_D current is observed and an important variation in the conductance in the saturation region is measured. In the case of source BD (down triangles) the after-HBD characteristics have the same shape as the fresh ones, but a strong reduction of V_{DSAT} and I_{DSAT} is observed. The BD MOSFET model has been used to quantify the variation of the transistor curves after HBD (continuous lines in figure 2). Note the good fitting of the transistor curves after source and drain HBD. The model has also been used to simulate the experimental transistor characteristics after oxide HBD in the channel [6] (not shown here).

To analyse the effect of the oxide degradation process previous to HBD on transistor characteristics, constant voltage stresses of 3.7V were applied to the gate of nMOSFETs (1.5V bulk technology, W/L ratio of 10μm/0.175μm and oxide thickness of 2.2 nm). The stress was applied during 3000 seconds to provoke a low level of damage in the oxide (the gate currents through the

oxide were of the order of nA). The degradation was produced between gate and source (source BD). Figure 3 shows the effect of this stress on the transistor curves. A reduction of the I_{DSAT} is observed although the decrease is not so important as for the case of oxide HBD. For this degradation level, the I_D-V_G transistor curve (Figure 4) shows an increase of the threshold voltage. The fresh and damaged transistor characteristics have been fitted in this case using the BSIM4 model. Good fittings of the curves have been obtained (continuous lines in figure 3 and 4). However, the number of model parameters needed to fit the curves is higher than that used with the BD MOSFET model which makes the extraction parameters more complicated.

In this work, the effect of oxide degradation and HBD on transistor characteristics has been analysed. For similar BD hardness the output characteristics are strongly affected by the BD location. In case of drain HBD negative I_D current has been observed and a large modification in the conductance in the saturation region is measured. For source BD the I_D-V_{DS} curves have the same shape of the fresh one but a reduction in the saturation level is observed, stronger for oxide HBD. Two different models have been used to fit the transistor curves with oxide degradation and breakdown: the BD MOSFET model and the BSIM4. Although the second one is more accurate, the number of parameters needed to model the transistor is larger. Both of them are able to take into account the effect of the oxide degradation and BD on the device characteristics. This is crucial to develop accurate transistor models to be included in a circuit simulator.

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References:

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Figures:

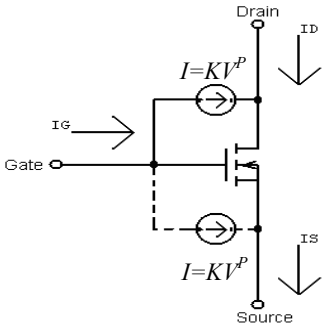

Fig. 1. Schematics of the BD MOSFET model. The output characteristics of the transistor are described by the nth power MOSFET model. The voltage controlled current sources take into account the additional BD current through the gate.

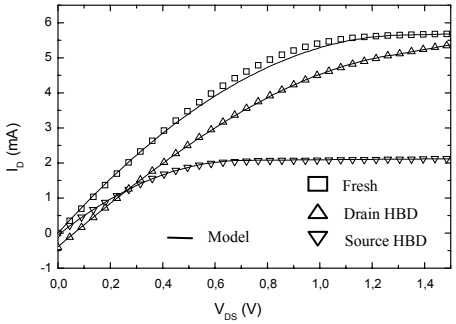

Fig. 2. I_D-V_{DS} curves measured for V_G=1.5V for a fresh transistor and after drain and source HBD. W/L ratio = 20µm/0.6µm. Continuous lines correspond to the fitting of the data to the BD MOSFET model.

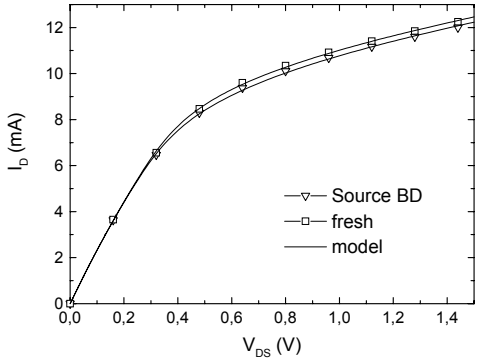

Fig. 3. I_D-V_{DS} curves for V_G=1.5V for a fresh transistor and after a low level of oxide degradation between gate and source. W/L ratio = 10µm/0.175µm. Continuous lines correspond to the fitting of the curves with the BSIM4 model.

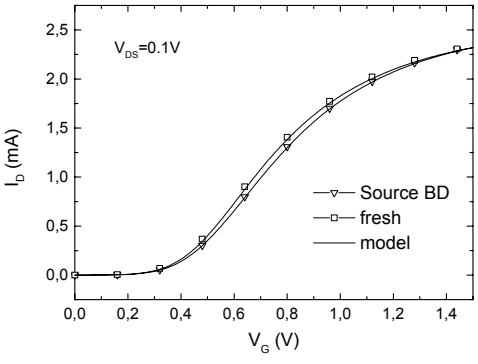

Fig. 4. I_D-V_G curves for a fresh transistor and for the oxide degradation level between gate and source shown in figure 3. An increase of the threshold voltage is observed after the oxide degradation.