NANOPHOTONIC WAVEGUIDES IN SILICON-ON-INSULATOR FABRICATED WITH CMOS TECHNOLOGY

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In the last decade, optical communication has been one of the driving forces behind the rapid expansion of the Internet, providing the huge bandwidths needed for the explosively increasing data traffic. However, when compared to the ultralarge-scale integration of complementary metal–oxide–semiconductor (CMOS) circuits, the optical components used for routing and switching in fiber-optical links are large and primitive looking, and the larger part of the functionality is still performed in the electrical domain, requiring many electrooptical conversions.

In recent years, more and more functions are being implemented optically and combined into photonic integrated circuits (PICs). Still, current PICs combine only a limited number of functions on a single chip, as large areas are required just to guide the light from one functional element to another through waveguides. In particular, waveguide bends prove a crucial limitation, as the bend radius needs to be adequately large to prevent radiation losses.

Therefore, to increase the level of integration in PICs, it is not only necessary to scale down the individual functional elements, but also reduce the area required for waveguiding. This requires narrow waveguides that can have tight bends with little loss.

In recent years a new technology has been emerging from research labs worldwide: the use of standard Silicon-on-Insulator (SOI) wafers and standard Silicon processing technologies to create ultra-compact so-called nanophotonic components and circuits in Silicon [1]. See Figure 1.

The term nanophotonic calls for some interpretation. The typical smallest feature sizes – widths, thicknesses, lengths – in wavelength-scale photonic structures are in the range of one tenth of a wavelength to one wavelength. For operation at a wavelength of 1550 nm for example – corresponding to a wavelength in Silicon of about 500 nm – the required smallest feature sizes are typically between 50 and 500 nm. This matches nicely the capabilities of present day's CMOS technology. However, the accuracy and reproducibility of the spectral behaviour of the optical functions are directly correlated to the geometric accuracy of these features in the device. As a rule of thumb one can say that a spectral accuracy of 1 nm (relative to a wavelength of 1550 nm) translates into a geometric accuracy of 1 nm (relative to a feature size of 50-500 nm).

For research purposes, the most used pattern definition technique is e-beam lithography. However, this technique is not suitable for mass manufacturing, as it is a serial and, therefore, slow process. Classical photolithography, used for the fabrication of the current generation of PICs, lacks the resolution to fabricate these submicrometer structures. Deep ultraviolet (UV) lithography is the continuation of optical lithography into the deep UV wavelengths range. With illumination wavelengths of 248 nm or less, this technique offers both the resolution and the speed required for the mass manufacturing of PICs with submicrometer features [1]. Furthermore the high-index contrast interfaces in these devices need to be smooth down to the 1 nm level to avoid scattering losses.

The scattering at interface is the most relevant loss factor. Reducing scattering losses requires careful process optimization to reduce sidewall roughness. In literature, values varying from

11 nm to 2 nm have been reported for the roughness standard deviation resulting in a corresponding reduction in losses from over 100 dB/cm to below 4 dB/cm for single mode waveguides [2].

The Public University of Navarre is currently developing a new measurement strategy for the estimation of the roughness parameters root mean square (*rms*) and autocorrelation length (L_c) of integrated waveguides based on the surface light scattering method [3] (Figure 2). Preliminary results show the concept is applicable to photonic waveguides although future optimization is required for its applicability to nanophotonic components.

References:

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Acknowledgments: This work has been supported by Spanish CICYT under project TEC 2004-05936-C02-01/MIC.

Figures:

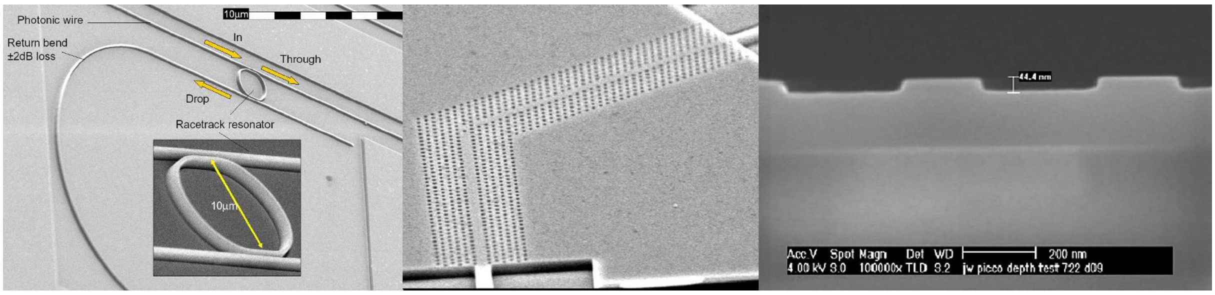

Figure 1: Nanophotonic components, ring resonator, photonic crystal and in plane fiber coupler.

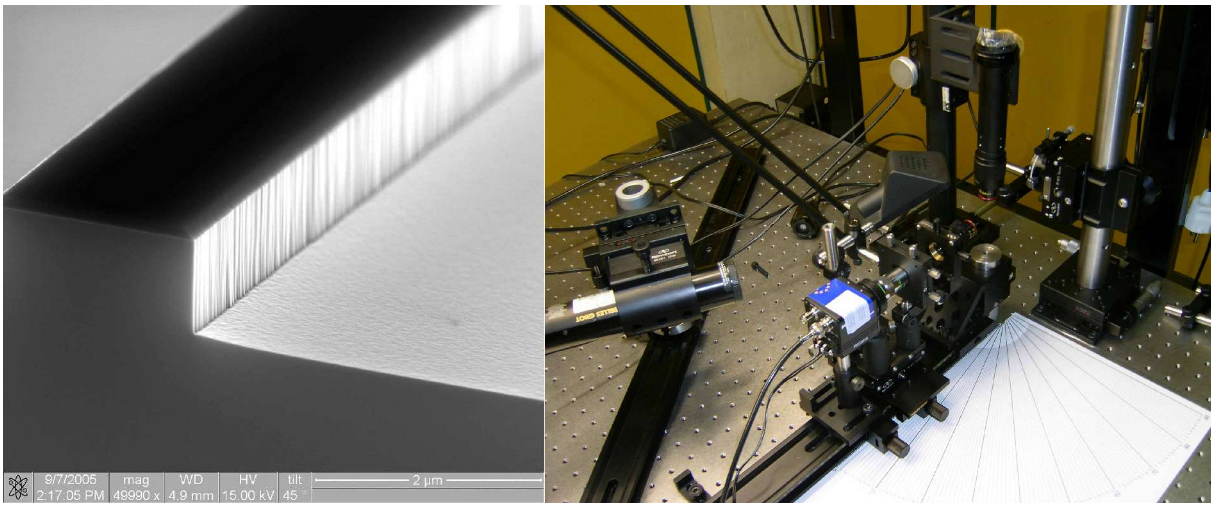

Figure 2: Roughness at the side of a photonic waveguide, and experimental setup for the estimation of the roughness random parameters *rms* and L_c.