

# Contacting single carbon nanotubes by e-beam lithography

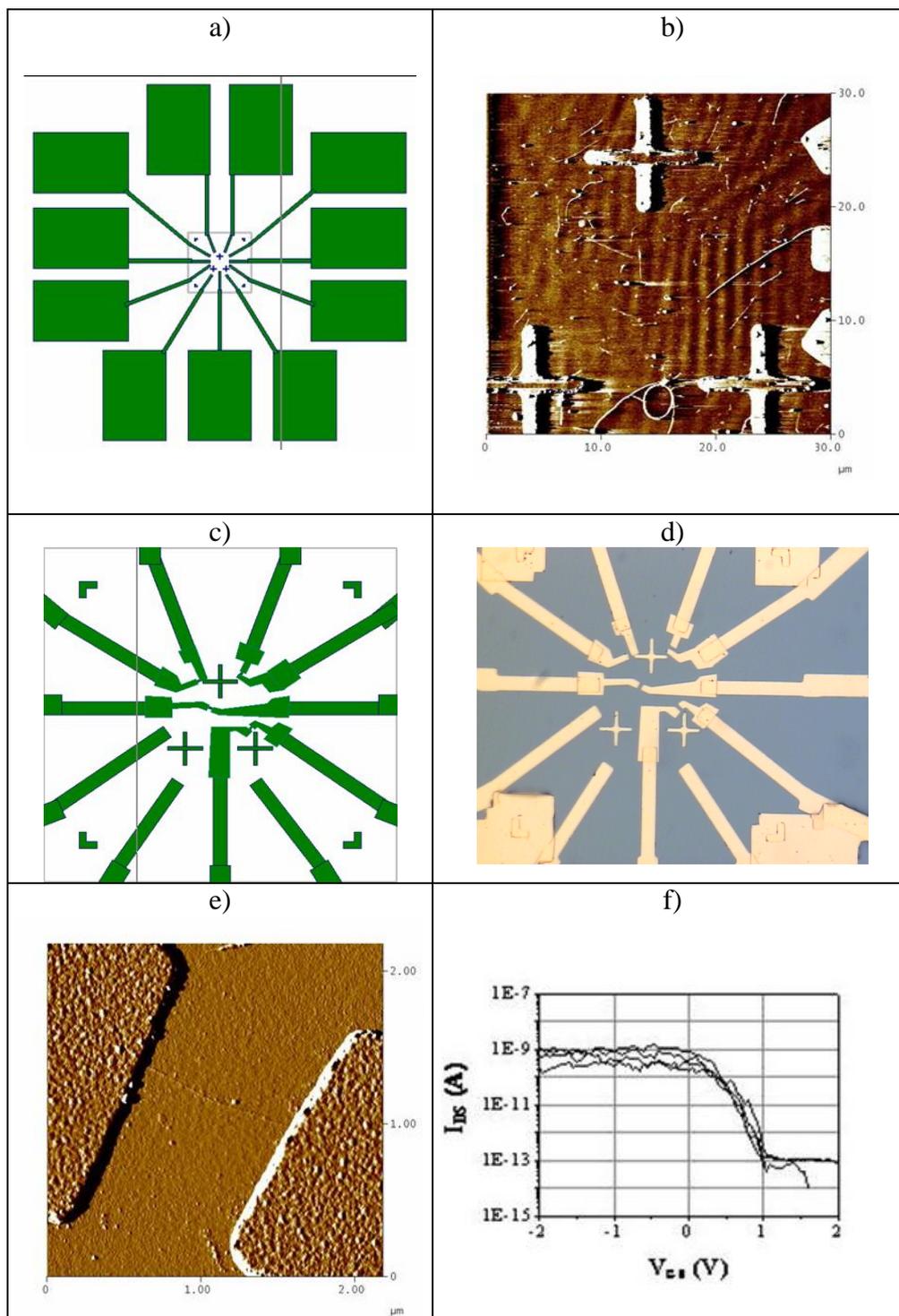
Gemma Rius, Servane Blanqué, Xavier Borrisé, Adrian Bachtold and Francesc Pérez- Murano  
Institut de Microelectrònica de Barcelona (CNM-CSIC). Campus UAB 08193  
Bellaterra (Spain)  
[gemma.rius@cnm.es](mailto:gemma.rius@cnm.es)

Since the discovery of carbon nanotubes (CNT), many research groups have been exploring their thermal, electronic and mechanical properties for multiple applications. Single walled carbon nanotubes (SWNT) are one-dimensional conductors with metallic or semiconducting behaviour, depending on their chirality. Semiconducting SWNTs have attracted a lot of interests as they can define conductive channels of field-effect transistors (CNTFET). Such devices are widely used as ultra-sensitive sensors.

In this communication, we present the process at IMB-CNM for the fabrication of CNTFETs using electron beam lithography (EBL). The starting substrate is a 200 nm thermally grown silicon oxide layer on a silicon wafer. Device fabrication starts with the definition of the marks that will act as reference points to locate the nanotubes by means of AFM inspection, and the definition of the pads and contact lines to perform the electrical characterization (Figure 1.a). The EBL process consists on exposing a thin layer of PMMA (120 nm), which is developed using MIBK:IPA (1:3). Then, a thin chromium (5 nm) plus gold (45 nm) layer is deposited on the sample. A lift-off process removes the remaining PMMA leaving the metal pattern on the surface. CNT are then deposited on the surface from a solution using spinning. AFM inspection is performed to determine the position of the nanotubes (figure 1.b) with respect to the previous defined marks. This information is used for the second EBL design to contact the nanotubes (figure 1.c). A double layer of PMMA (100 nm of PMMA 495K MW and 120 nm of PMMA 950K MW) is then deposited on the sample, exposed and developed. The resulting pattern is transferred by evaporating chromium and gold and a subsequent lift off process (figure 1.d). The alignment procedure is successful as it can be observed in figure 1.e.

Electrical characterization reveals the performance of the devices. We have used a probe station and a semiconductor parameter analyzer (HP4155B). Figure 1.f shows an example of a CNTFET characteristic with an On/Off current ratio of  $10^4$ , which has been operative for several months. CNTFET devices fabricated in this way are going to be used to perform electrical transport studies, as well as to fabricate (bio)chemical sensors.

This work has been partially financed by projects Sensonat (NAN2004-09306-C05-01) and Charpan (NMP2-CT-2005-515803).



**Figure 1.** a) Marks, pads and contact lines design; b) AFM inspection after the CNT deposition; c) Contact design; d) Optical image after the second EBL process and lift-off. e) AFM image of a resulting contacted nanotube; f) Electrical characterization ( $V_{sd}=0.15-0.30$  V).