Fabrication of arrays of silicon nanowires

X. Cartoixà,[1,*] Y. Gebremichael,[1,2] A. Sánchez,[2] X. Borrisé,[2,3] R. Rurali,[4] J. Suñé,[1] M. Schmidt,[4] M. I. Alonso,[4] A. R. Goñi,[4] and F. Pérez-Murano[2]

[1] *Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, 08193 Bellaterra, Barcelona, Spain*

[2] *Institut de Microelectrònica de Barcelona CNM-IMB (CSIC), 08193 Bellaterra, Barcelona, Spain*

[3] *Institut Català de Nanotecnologia – CIN2 (CSIC-ICN), 08193 Bellaterra, Barcelona, Spain*

[4] *Institut de Ciència de Materials de Barcelona ICMAB (CSIC), 08193 Bellaterra, Barcelona, Spain*

Silicon nanowires (SiNWs) hold great promise to integrate conventional Si devices in future nanoelectronics applications [1], and their use as bipolar transistors, logic gates, non-volatile memories, solar cells, biological sensors and energy conversion devices has been reported. Most of these applications demand a high level of positioning control and homogeneity regarding the electrical (doping profile) and morphological (eg. length, diameter, crystalline orientation) properties, which can be easily achieved with top-down fabrication methods.

We have recently proposed a fabrication strategy for arrays of nanowires based on the nanopatterning of holes into a substrate [2]. Calculations show that the electronic states are located preferentially at the interstitial part between the holes, and the degree of coupling between these preferential locations could be tuned at fabrication time from an array of isolated quantum wire states, Fig. 1.(a), to a strongly coupled artificial solid built from nanowires, Fig. 1.(b). This method of fabrication benefits, of course, of all the advantages of the top-down nanofabrication methods mentioned above and, in addition, its exclusive features include the variable tuning degree of the electronic coupling between the wire states, the superior mechanical stability of the nanostructure and, most importantly, a typical wire size limited by the positioning precision of the used lithography technique rather than the minimum dot size. There exists experimental indication that this approach might be feasible, since an analogous behavior at the intersection between reduced dimensionality heterostructures, the so-called T-shaped quantum wires, was first verified almost two decades ago [3].

A project has been recently started to experimentally demonstrate these effects [4]. With a combination of electron beam lithography and a specially developed reactive ion etching process, holes with diameters from 30 nm up to 600 nm, and pitch from 90 nm up to 1000 nm (Fig. 2) were fabricated, achieving no observable scalloping [5]. In order to reduce the size of interconnects and interstitials, the sample has been thermally oxidized, and afterwards the silicon oxide was removed by HF acid (Fig. 3). Quantum confinement effects have been probed by photoluminescence (PL). Measurements were performed with a 488 nm laser source and a high throughput spectrometer equipped with confocal microscope in a wide spectral range from near infrared (900 nm) up to 400 nm, observing the presence of a PL peak reminiscent of those appearing in Si nanocrystals embedded in SiO_2 matrices, a first indication that the interstitials are supporting quantum-confined states.

We acknowledge the financial support of the Spanish Ministerio de Ciencia e Innovación under contract No. TEC2008-01865-E.

*Electronic address: Xavier.Cartoixa@uab.es

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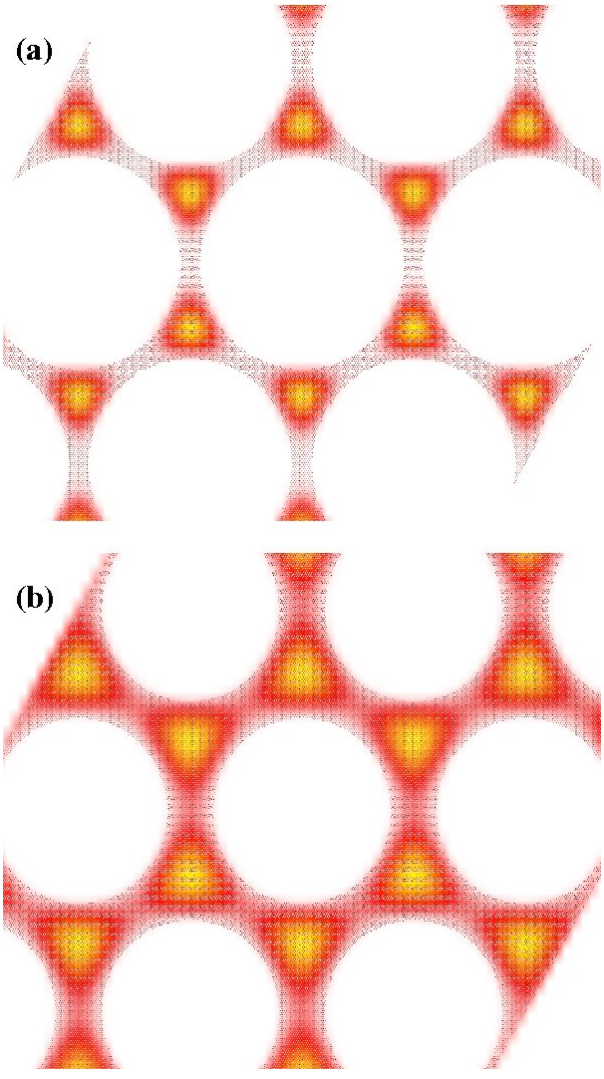

FIG. 1: GaAs substrate, (a) interconnect thickness ∼3.2 nm and hole diameter ∼37.2 nm and (b) interconnect thickness ∼8.4 nm and hole diameter ∼32.0 nm: charge density corresponding to the bottom of the conduction band state, featuring (a) independent and (b) coupled nanowire behavior.

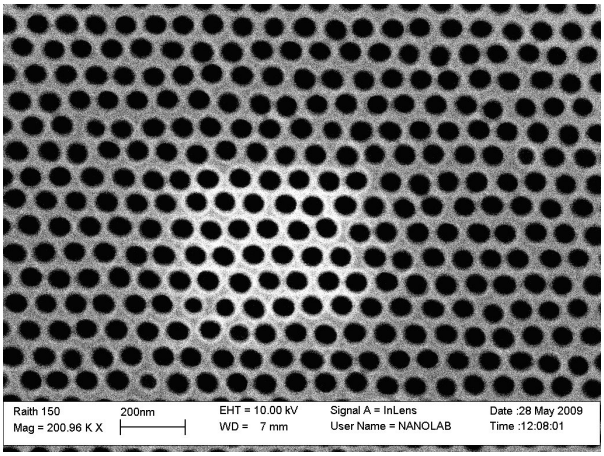

FIG. 2: 70 nm diameter holes with a 100 nm pitch on a silicon substrate.

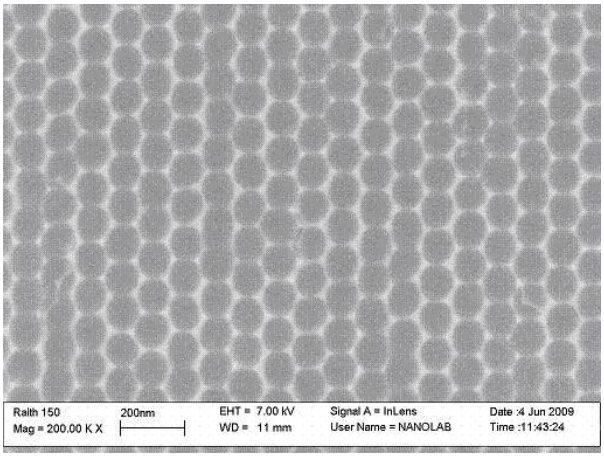

FIG. 3: 70 nm diameter holes with a 100 nm pitch on a silicon substrate, after thermal oxidation and removal by HF.